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Pillsbury Winthrop LLP  
Intellectual Property Group  
Suite 2800  
725 South Figueroa Street  
Los Angeles, CA 90017-5406

EXAMINER

WOODS, ERIC V

ART UNIT

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Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/766,636	<b>Applicant(s)</b> YOSHIDA, YOSHIJI	
	<b>Examiner</b> Eric V. Woods	<b>Art Unit</b> 2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 January 2004.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 January 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

*By*

## **DETAILED ACTION**

### ***Specification***

The abstract of the disclosure is objected to because the construction "wherein it" is utilized on the third line in a manner that is confusing, wherein that phrase should simply be replaced with "which". Correction is required. See MPEP § 608.01(b).

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Synchronized Sprite Rendering with Sprite Buffer.

The incorporation of essential material in the specification by reference to an unpublished U.S. application, foreign application or patent, or to a publication is improper. Applicant is required to amend the disclosure to include the material incorporated by reference, if the material is relied upon to overcome any objection, rejection, or other requirement imposed by the Office. The amendment must be accompanied by a statement executed by the applicant, or a practitioner representing the applicant, stating that the material being inserted is the material previously incorporated by reference and that the amendment contains no new matter under 37 CFR 1.57(f). Specifically, the priority documents should be referenced but cannot be incorporated into the specification by reference. Further, there is nothing to incorporate by reference; such documents are entirely in Japanese.

The specification is objected to because it does not describe the "END" function in Figures 2 and 3, which leads off of block / step Sa1 as described on page 7 of the

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instant specification. The specification also does not set forth when the process actually ends.

The specification is also objected to because it does not explain Figure 6, except at the bottom of page 13, and does not explain the relevancy of the timing diagrams therein.

Applicant is reminded that no new matter may be introduced in such amendments.

### ***Priority***

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file. .

### ***Information Disclosure Statement***

The information disclosure statement (IDS) submitted on 28 January 2004 was filed with the instant application. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the examiner is considering the information disclosure statement.

### ***Drawings***

Figure 7 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated, evidence of this being found on pages 1-2 of applicant's specification, particularly the mention of Figure 7 in the "Description of the Related Art" section on page 1. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the

page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the elements not mentioned in the description: The significance of the timing diagrams in Figures 6A-6E is not explained in the specification, particularly not for 6B-6E. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

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Claims 8-9 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for having read and write signals synchronized, does not reasonably provide enablement for reading data from the frame buffer when writing does not take place to the sprite buffer. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention commensurate in scope with these claims. Specifically, the parent claims (6 and 7) specify that the display controller is synchronized such that display data is read from the second storage (frame buffer) at a time data is written to the first storage (sprite buffer). However, claims 8 and 9 appear to contradict that by specifying that read operations take place when sprite data are not written to the first buffer, such that this would seem to violate the imposed synchronization by the display controller.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

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4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 1 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Blossom et al (US 5,892,521)('Blossom') in view of Witzig et al ("E787 Technical Note #264". C. Witzig, S. Adler. 1993).

As to claim 1,

An image processing device comprising:

-A decoder for decoding compressed image data representing sprite patterns so as to restore original sprite pattern data; (Blossom 3:9-22; use of coding and coding schema is notoriously well known in the art, both to prevent illegal copying of data from ROMs and the like, and to prevent its use if copied, and to provide proprietary formats that will enable only one format or type of data ROM to interact correctly with a system. Also, coding is notoriously well known in the art to increase efficiency. Blossom provides hardware for decoding and decompressing such data, and the entire purpose of decompression and decoding is to return the data to its original form)

-A write controller for writing the sprite pattern data into a first storage; (3:23-36 (note that data processor 48 writes sprites to memory); 6:20-55 and Figure 6, where a sprite management system exists that writes sprites to sprite buffers 122 in sprite memory 116, where the sprite management system constitutes a write controller—the sprite memory is read/write – RAM –5:55-60)

-A read controller for reading the sprite pattern data from the first storage; (5:55-60, sprite memory 116 is read/write RAM, with sprite buffers 122 in Figure 6. 6:64-7:15 sets forth methods for writing data from sprite buffers 122 to frame buffer 118. Prima facie, if

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data is written from one buffer to another it very clearly must be read from the first one before it can be written to another)

-A processing controller for performing prescribed processing on the sprite pattern data read from the first storage and for writing processed data into a second storage as display data; and (Data processor 112 in Figure 6 executes the method of Figure 7 (see 7:40-8:6, which performs depth-based processing on the sprite pattern data from the first storage and writes it to the second storage; further, data processing system can take in video streams and handle video sprites – 8:50-9:5—where chroma-key processing is performed on data from sprite buffers 122 in sprite memory 116 by data processor 112 as well as on pixels in frame buffer 118. Therefore, it is proven that data processor 112 serves as the recited 'processing controller' and also moves data read from sprite buffers 122 in sprite memory 116 to frame buffer 118 as stated in the above-cited locations in the reference – 9:1-6 states, *inter alia*, "Data processor **112** also forms transfer means for writing or transferring pixel values from the sprite buffer to the display frame compositional buffer".)

-A display controller for reading the display data from the second storage so as to output the read display data to a display, (Display processor 108 in VGA compatible subsystem 106, where the display processor 108 reads from frame buffer 110 (5:15-5:55) and then outputs such data to a display (5:32-52, where the display processor continuously and repetitively generates values to create driver signals at levels appropriate to produce the contents of the frame buffer 110 on the screen 115 of display device 104.)



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-Wherein the write controller and the read controller perform write and read controls on the first storage to serve as a first-in-first-out memory. (Witzig pages 1-2, where it is stated that a FIFO is a ring buffer with a read and write pointer. FIFOs reside in shared memory and any process after an initial attachment to the FIFO system can read and write into any FIFO (e.g. sprite buffer, since sprite buffers are in shared memory (RAM)). Further, semaphore operations can be implemented that guarantee that only one process accesses one FIFO at a time. FIFOs implemented in this manner have several advantages for event distribution among an arbitrary number of processes: once an event is in the FIFO, only an object or structure is passed between processes. Once a process takes such a structure out of a FIFO, it is guaranteed that no other process can access this object by mistake. A CPU intensive stage can be done by several processes in parallel, and many other options as stated therein)

Blossom teaches all the limitations of this claim except expressly advocating the use of a FIFO for the first storage. The use of a FIFO for such storages is well known in the art – see for example Kajiya et al (US 5,977,977)(25:20-45, 26:63-27:5, 27:40-50, and many other locations) – in systems that implement sprite engines (mostly assigned to Microsoft), as is Blossom. Furthermore, FIFOs have many advantages as set forth above in summary from the Witzig reference. For those reasons, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the first storage (the sprite buffers) to be FIFOs as per Witzig (whether implemented in software as per Witzig, or in hardware, as would be obvious (Kajiya or otherwise)) as recited in the claim above.

Additionally, Witzig is analogous art, in that it is directed to methods of implementing software FIFO buffers for graphics purposes, which means that it has relevance to the instant application, and motivations as above, since Blossom is implemented as a mix of software and hardware, particularly the sprite management system (3:60-4:5).

Claims 2 and 5 are rejected under 35 U.S.C. 103(a) as unpatentable over Blossom and Witzig as applied to claim 1, and further in view of Bromley et al (US 4,672,541).

As to claim 2, this claim is identical to claim 1, the rejection to which is incorporated by reference in its entirety, with various additional limitations, namely:

-A memory for storing compressed image data representing sprite patterns; (Bromley Figure 3, cartridge ROM 24 stores "specific video images" (7:30-32), which are obtained from the cartridge ROM (6:37-40, 48-52), which are known to be images of players (7:14-22), and video images within the system of Bromley are known as "sprites" (5:4-8), since the images of the players are inherently movable and are supplied from ROM with offset coordinates (7:14-22). Such players are clearly sprites (8:28-31).)(Blossom clearly teaches that sprite data can be compressed (3:20-22), and that it can be obtained from non-volatile storage (3:12-16))

-A sprite attribute table for storing sprite attribute data representing attributes of the sprite patterns. (Bromley teaches the use of sprite attribute tables in (5:3-35), where each sprite has an entry in a sprite attribute table, as in Figure 4 for example (element

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34), with attributes such as location and color. Such table is initially loaded from ROM into RAM (Bromley 8:10-17).

-A decoder for reading the compressed image data from the memory and for decoding the read compressed image data to restore original sprite pattern data before compression with reference to the sprite attribute data stored in the sprite attribute table ((Blossom 3:9-22; Blossom states that the hardware is provided to **receive** data, where if the data is a non-volatile storage mechanism, this inherently requires reading the data. Blossom further teaches decompression and decoding of data, as explained in claim 1, and the entire purpose of such activities are to recover the original data.)(Bromley clearly loads such sprites as are listed in the attribute table from ROM, since the attribute table is clearly loaded **from** ROM, which means that the data is clearly being restored with respect to the sprites in the attribute table, and their pattern is clearly one of their properties (such as color for example in Figure 4).

Blossom and Witzig do not expressly teach all of the limitations of the above claim, except that Blossom teaches that sprite pattern data may be compressed and stored on non-volatile storage (e.g. ROM). Compression is an obvious expedient because it allows more data to be stored on a ROM, and thusly the amount of memory required is less. Compression is also notoriously well known in the art, and since the primary references states that it can be used in conjunction with a ROM, no further explanation is needed.

Bromley is clearly analogous art, as it teaches sprite data stored on non-volatile memory and means for accessing that for purposes of video games (which is clearly

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analogous art with the instant application). It uses sprites for the purposes of computer graphics, particularly video games, and thusly would be analogous art with Blossom as well. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the video games and memory management systems of Bromley with Blossom and Witzig, since Bromley clearly teaches that the video game system has improvements over the prior art, particularly in presenting different views of a playfield together (2:43-57), where it is clear that the system of Blossom is intended to generate graphics from external sources, but those external sources are never specified, nor are the access methods. The system of Bromley would provide both the external source of sprites and a method to access them and put them into the first storage of Blossom. Finally, the use of such sprite attribute tables is notoriously well known in the art for obtaining data from ROMs (see for example JP 2002-341859 and JP 59-111067, see attached DERWENT abstracts.)

As to claim 5, this claim is merely a method with steps corresponding to exact sections of the apparatus of claim 2. The arrangement of the clauses is slightly different, but the limitations are otherwise the same. As such, the rejection to claim 2 is incorporated by reference and properly applied to claim 5.

Claim 3 is rejected under 35 U.S.C. 103(a) as unpatentable over Blossom and Witzig as applied to claim 1, and further in view of Kitahara et al (US 5,634,850).

As to claim 3,

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An image processing device according to claim 1, wherein the prescribed processing correspond to rendering actualizing at least one of magnification, reduction, rotation, and deformation with respect to the sprite pattern data.

Blossom and Witzig do not expressly teach that the prescribed processing corresponds to such operations as above. Kitahara, an analogous art (directed to rendering sprites and the like, see Figure 1 with the sprite engine, and the Abstract), clearly teaches that the sprite engine clearly reads out image data (such as a character) and carries out processes for the read images such as rotation, enlargement, reduction, and/or color compensation processes (3:59-63), thusly proving that it is obvious to perform such processing when such data is transferred from the first storage to the second storage, since Kitahara initially stores sprites in sprite VRAM 22, and then performs such transformation processing before the data is transferred to sprite frame buffer 23 which is known to hold at least one picture (e.g. frame buffer) – see 3:25-30 and 3:59-63, which when read means that characters are read out of the sprite VRAM 22 (first storage), processed, and sent to sprite frame buffer 23 (second storage) – see Figure 12 or 1 for example.

It would have been obvious to one of ordinary skill in the art to combine the system of Kitahara with Blossom and Witzig, since Kitahara provides a more efficient way for processing motion in a system employing sprites (1:50-67).

Claim 4 is rejected under 35 U.S.C. 103(a) as unpatentable over Blossom, Witzig, and Bromley as applied to claim 2, and further in view of Kitahara et al (US 5,634,850).

As to claim 4,

An image processing device according to claim 2, wherein the prescribed processing correspond to rendering actualizing at least one of magnification, reduction, rotation, and deformation with respect to the sprite pattern data.

Blossom, Witzig, and Bromley do not expressly teach that the prescribed processing corresponds to such operations as above. Kitahara, an analogous art (directed to rendering sprites and the like, see Figure 1 with the sprite engine, and the Abstract), clearly teaches that the sprite engine clearly reads out image data (such as a character) and carries out processes for the read images such as rotation, enlargement, reduction, and/or color compensation processes (3:59-63), thusly proving that it is obvious to perform such processing when such data is transferred from the first storage to the second storage, since Kitahara initially stores sprites in sprite VRAM 22, and then performs such transformation processing before the data is transferred to sprite frame buffer 23 which is known to hold at least one picture (e.g. frame buffer) – see 3:25-30 and 3:59-63, which when read means that characters are read out of the sprite VRAM 22 (first storage), processed, and sent to sprite frame buffer 23 (second storage) – see Figure 12 or 1 for example.

It would have been obvious to one of ordinary skill in the art to combine the system of Kitahara with Blossom and Witzig, since Kitahara provides a more efficient way for processing motion in a system employing sprites (1:50-67), and Bromley teaches a video game, as does Kitahara, and the system of Kitahara would make the motion effects of Bromley more realistic (1:50-67).

Claims 6, 8, and 12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Blossom et al (US 5,892,521)('Blossom') in view of Yamashita et al (US 6,313,844 B1) and Takahashi (JP 40-3249888A (patent), JP 02-047647 (application)).

As to claims 6 and 12, (apparatus, with method having the exact same limitations as steps as there elements in the apparatus)

An image processing device comprising:

-A decoder for decoding compressed image data representing sprite patterns so as to restore original sprite pattern data; (Blossom 3:9-22; use of coding and coding schema is notoriously well known in the art, both to prevent illegal copying of data from ROMs and the like, and to prevent its use if copied, and to provide proprietary formats that will enable only one format or type of data ROM to interact correctly with a system. Also, coding is notoriously well known in the art to increase efficiency. Blossom provides hardware for decoding and decompressing such data, and the entire purpose of decompression and decoding is to return the data to its original form)

-A write controller for writing the sprite pattern data into a first storage; (3:23-36 (note that data processor 48 writes sprites to memory); 6:20-55 and Figure 6, where a sprite management system exists that writes sprites to sprite buffers 122 in sprite memory 116, where the sprite management system constitutes a write controller—the sprite memory is read/write – RAM –5:55-60)

-A read controller for reading the sprite pattern data from the first storage; (5:55-60, sprite memory 116 is read/write RAM, with sprite buffers 122 in Figure 6. 6:64-7:15 sets forth methods for writing data from sprite buffers 122 to frame buffer 118. Prima facie, if

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data is written from one buffer to another it very clearly must be read from the first one before it can be written to another)

-A processing controller for performing prescribed processing on the sprite pattern data read from the first storage and for writing processed data into a second storage as display data; and (Data processor 112 in Figure 6 executes the method of Figure 7 (see 7:40-8:6, which performs depth-based processing on the sprite pattern data from the first storage and writes it to the second storage; further, data processing system can take in video streams and handle video sprites – 8:50-9:5—where chroma-key processing is performed on data from sprite buffers 122 in sprite memory 116 by data processor 112 as well as on pixels in frame buffer 118. Therefore, it is proven that data processor 112 serves as the recited 'processing controller' and also moves data read from sprite buffers 122 in sprite memory 116 to frame buffer 118 as stated in the above-cited locations in the reference – 9:1-6 states, *inter alia*, "Data processor **112** also forms transfer means for writing or transferring pixel values from the sprite buffer to the display frame compositional buffer".)

-A display controller for reading the display data from the second storage so as to output the read display data to a display, (Display processor 108 in VGA compatible subsystem 106, where the display processor 108 reads from frame buffer 110 (5:15-5:55) and then outputs such data to a display (5:32-52, where the display processor continuously and repetitively generates values to create driver signals at levels appropriate to produce the contents of the frame buffer 110 on the screen 115 of display device 104.)



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-Wherein the display controller realizes synchronization such that a timing for writing the sprite pattern data into the first storage is synchronized with a timing for reading the display data from the second storage. (Yamashita (9:5-3) teaches that timing commands between a first and second memory are synchronized such that read and write operations occur opposite to each other as stated in the above claim, and teaches that such synchronization is clearly beneficial because it allows read and write operations to occur in parallel. The overall system of Yamashita is clearly directed to a method of synchronizing read and write signals, and prior art performs such steps as well, where such synchronization is performed because it is more efficient and more economical)(Takahashi teaches that synchronizing read and write signals results in a more economical memory.)

Blossom teaches all the limitations of this claim except expressly teaching that the timing for writing data into the first storage is synchronized with a timing for reading data from the second storage. Yamashita (9:5-29) and Takahashi clearly teach that this technique is beneficial for various reasons. Therefore, in light of the prior art, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Blossom to synchronize the writing to the first memory and reading from the second memory for at least the above reasons, and because it would be trivially obvious to one of ordinary skill in the art that maximizing the duty cycle of the two memories so that they spend most of their time in transfer mode rather than blocking each others data would be beneficial (maximization of duty cycle and transfer rate as notoriously well known expedient).

As to claim 8,

The references do not expressly teach all limitations. The rejection to claim 6 is incorporated by reference.

As to the limitation that the display controller starts to read the display from the second storage at a timing that allows the display data of one line to be read out, Blossom teaches that the display device utilized is a conventional CRT display, which scans one line at a time, top to bottom (1:15-50), and the preferred embodiment (e.g. example) utilizes a CRT (1:50-67). Therefore, Blossom inherently teaches that the display controller would read data one line at a time from the frame buffer (Yamashita teaches the use of line buffers anyway, which would teach a line by line read in any case). Also, inherent in the way CRTs operate is that there is are Vsync and Hsync (vertical and horizontal synchronization) signals that, in order to be displayed correctly, the display device must match the vertical and horizontal write rates set by those sync signals, or else convert those signals to another video format with different sync rates that match that of the monitor. The VGA standards family uses a common sync rate, and most monitors therefore support that mode, where lines are read from the frame buffer and written to the display at a rate specified by the Vsync signal. This may be modified (as in Yamashita) by using line buffers or the like, as is trivially well known in the art, and it would be obvious to do so (if necessary) as set forth in Yamashita, which is already part of the rejection.

As to the limitation that the reading "is counted backwardly from a start timing of a horizontal display period of the device", the Hsync (or horizontal synch) signal for a

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display device sets the rate of reading from one line of the display and thusly sets the rate of counting. The start timing provided by the elapse of one time period between Vsync signals causes a new start signal for reading a new line of the frame buffer, and that signal constitutes 'a horizontal display period of the device'. As to the limitation of reading backwards, this is a matter of design choice (see *In re Gazda*, 219 F.2d 449, 104 USPQ 400 (CCPA 1955)) where the direction of reading is a moot point (reversal of parts as obvious expedient). Reading right to left or left to right provides no technical advantages, and there have been many displays and hardware that read in both directions. Further, depending on the nature of the memory and computer (e.g. whether or not the system was big-endian or little-endian), it might be read in reverse order anyway. Therefore, this limitation is meaningless.

As to proof of both of the above, see Giloi (Wolfgang K. Giloi. "Interactive Computer Graphics: Data Structures, Algorithms, Languages". Pages 246-248). Further see Broemmelsiek (US 5,574,836)(7:1-12, 18:62-19:10) and Hannah (US 5,345,252)(2:3-15,7:65-8:67) for proof that both of the above are old and well known in the art.

As to the limitation that "in a time period in which the sprite pattern data is not written to the first storage, the display controller starts to read..." the display **must** operate in the manner specified above. It is inherent to the operation of a CRT that the display controller will read data at a given timing, and in CRTs, the data is pulled from the frame buffer, regardless of what the first storage is doing. (Also, there are enablement problems with this wording, see above – it does not make sense that the

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display would read only when the sprite patterns are not written into the first storage).

But in any case, it is an obvious expedient that whenever there is bus latency, that data should be transferred in order to maximize use of the bus and available resources.

Obviously, transmitting the data in this 'down time' is old and well known in the art.

Therefore, the limitations of the above claim are met by the instant references and/or are rendered obvious, and/or shown to be implemented (or probably implemented) in holdings of inherency with respect to elements of the already-cited references.

Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as unpatentable over Blossom, Yamashita, and Takahashi as applied to claim 6, and further in view of Bromley et al (US 4,672,541).

As to claim 7, this claim is identical to claim 6, the rejection to which is incorporated by reference in its entirety, with various additional limitations, namely:

-A memory for storing compressed image data representing sprite patterns; (Bromley Figure 3, cartridge ROM 24 stores "specific video images" (7:30-32), which are obtained from the cartridge ROM (6:37-40, 48-52), which are known to be images of players (7:14-22), and video images within the system of Bromley are known as "sprites" (5:4-8), since the images of the players are inherently movable and are supplied from ROM with offset coordinates (7:14-22). Such players are clearly sprites (8:28-31).)(Blossom clearly teaches that sprite data can be compressed (3:20-22), and that it can be obtained from non-volatile storage (3:12-16))

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-A sprite attribute table for storing sprite attribute data representing attributes of the sprite patterns. (Bromley teaches the use of sprite attribute tables in (5:3-35), where each sprite has an entry in a sprite attribute table, as in Figure 4 for example (element 34), with attributes such as location and color. Such table is initially loaded from ROM into RAM (Bromley 8:10-17).

-A decoder for reading the compressed image data from the memory and for decoding the read compressed image data to restore original sprite pattern data before compression with reference to the sprite attribute data stored in the sprite attribute table ((Blossom 3:9-22; Blossom states that the hardware is provided to **receive** data, where if the data is a non-volatile storage mechanism, this inherently requires reading the data. Blossom further teaches decompression and decoding of data, as explained in claim 1, and the entire purpose of such activities are to recover the original data.)(Bromley clearly loads such sprites as are listed in the attribute table from ROM, since the attribute table is clearly loaded **from** ROM, which means that the data is clearly being restored with respect to the sprites in the attribute table, and their pattern is clearly one of their properties (such as color for example in Figure 4).

Blossom, Yamashita, and Takahashi do not expressly teach all of the limitations of the above claim, except that Blossom teaches that sprite pattern data may be compressed and stored on non-volatile storage (e.g. ROM). Compression is an obvious expedient because it allows more data to be stored on a ROM, and thusly the amount of memory required is less. Compression is also notoriously well known in the art, and

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since the primary references states that it can be used in conjunction with a ROM, no further explanation is needed.

Bromley is clearly analogous art, as it teaches sprite data stored on non-volatile memory and means for accessing that for purposes of video games (which is clearly analogous art with the instant application). It uses sprites for the purposes of computer graphics, particularly video games, and thusly would be analogous art with Blossom as well. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the video games and memory management systems of Bromley with Blossom, Yamashita, and Takahashi, since Bromley clearly teaches that the video game system has improvements over the prior art, particularly in presenting different views of a playfield together (2:43-57), where it is clear that the system of Blossom is intended to generate graphics from external sources, but those external sources are never specified, nor are the access methods. The system of Bromley would provide both the external source of sprites and a method to access them and put them into the first storage of Blossom. Finally, the use of such sprite attribute tables is notoriously well known in the art for obtaining data from ROMs (see for example JP 2002-341859 and JP 59-111067, see attached DERWENT abstracts.)

As to claim 9,

The references do not expressly teach all limitations. The rejection to claim 7 is incorporated by reference.

As to the limitation that the display controller starts to read the display from the second storage at a timing that allows the display data of one line to be read out,

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Blossom teaches that the display device utilized is a conventional CRT display, which scans one line at a time, top to bottom (1:15-50), and the preferred embodiment (e.g. example) utilizes a CRT (1:50-67). Therefore, Blossom inherently teaches that the display controller would read data one line at a time from the frame buffer (Yamashita teaches the use of line buffers anyway, which would teach a line by line read in any case). Also, inherent in the way CRTs operate is that there is are Vsync and Hsync (vertical and horizontal synchronization) signals that, in order to be displayed correctly, the display device must match the vertical and horizontal write rates set by those sync signals, or else convert those signals to another video format with different sync rates that match that of the monitor. The VGA standards family uses a common sync rate, and most monitors therefore support that mode, where lines are read from the frame buffer and written to the display at a rate specified by the Vsync signal. This may be modified (as in Yamashita) by using line buffers or the like, as is trivially well known in the art, and it would be obvious to do so (if necessary) as set forth in Yamashita, which is already part of the rejection.

As to the limitation that the reading "is counted backwardly from a start timing of a horizontal display period of the device", the Hsync (or horizontal synch) signal for a display device sets the rate of reading from one line of the display and thusly sets the rate of counting. The start timing provided by the elapse of one time period between Vsync signals causes a new start signal for reading a new line of the frame buffer, and that signal constitutes 'a horizontal display period of the device'. As to the limitation of reading backwards, this is a matter of design choice (see *In re Gazda*, 219 F.2d 449,

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104 USPQ 400 (CCPA 1955)) where the direction of reading is a moot point (reversal of parts as obvious expedient). Reading right to left or left to right provides no technical advantages, and there have been many displays and hardware that read in both directions. Further, depending on the nature of the memory and computer (e.g. whether or not the system was big-endian or little-endian), it might be read in reverse order anyway. Therefore, this limitation is meaningless.

As to proof of both of the above, see Giloi (Wolfgang K. Giloi. "Interactive Computer Graphics: Data Structures, Algorithms, Languages". Pages 246-248). Further see Broemmelsiek (US 5,574,836)(7:1-12, 18:62-19:10) and Hannah (US 5,345,252)(2:3-15,7:65-8:67) for proof that both of the above are old and well known in the art.

As to the limitation that "in a time period in which the sprite pattern data is not written to the first storage, the display controller starts to read..." the display **must** operate in the manner specified above. It is inherent to the operation of a CRT that the display controller will read data at a given timing, and in CRTs, the data is pulled from the frame buffer, regardless of what the first storage is doing. (Also, there are enablement problems with this wording, see above – it does not make sense that the display would read only when the sprite patterns are not written into the first storage). But in any case, it is an obvious expedient that whenever there is bus latency, that data should be transferred in order to maximize use of the bus and available resources. Obviously, transmitting the data in this 'down time' is old and well known in the art.



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Therefore, the limitations of the above claim are met by the instant references and/or are rendered obvious, and/or shown to be implemented (or probably implemented) in holdings of inherency with respect to elements of the already-cited references.

As to claim 8,

The references do not expressly teach all limitations. The rejection to claim 6 is incorporated by reference.

As to the limitation that the display controller starts to read the display from the second storage at a timing that allows the display data of one line to be read out, Blossom teaches that the display device utilized is a conventional CRT display, which scans one line at a time, top to bottom (1:15-50), and the preferred embodiment (e.g. example) utilizes a CRT (1:50-67). Therefore, Blossom inherently teaches that the display controller would read data one line at a time from the frame buffer (Yamashita teaches the use of line buffers anyway, which would teach a line by line read in any case). Also, inherent in the way CRTs operate is that there is are Vsync and Hsync (vertical and horizontal synchronization) signals that, in order to be displayed correctly, the display device must match the vertical and horizontal write rates set by those sync signals, or else convert those signals to another video format with different sync rates that match that of the monitor. The VGA standards family uses a common sync rate, and most monitors therefore support that mode, where lines are read from the frame buffer and written to the display at a rate specified by the Vsync signal. This may be modified (as in Yamashita) by using line buffers or the like, as is trivially well known in

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the art, and it would be obvious to do so (if necessary) as set forth in Yamashita, which is already part of the rejection.

As to the limitation that the reading "is counted backwardly from a start timing of a horizontal display period of the device", the Hsync (or horizontal synch) signal for a display device sets the rate of reading from one line of the display and thusly sets the rate of counting. The start timing provided by the elapse of one time period between Vsync signals causes a new start signal for reading a new line of the frame buffer, and that signal constitutes 'a horizontal display period of the device'. As to the limitation of reading backwards, this is a matter of design choice (see *In re Gazda*, 219 F.2d 449, 104 USPQ 400 (CCPA 1955)) where the direction of reading is a moot point (reversal of parts as obvious expedient). Reading right to left or left to right provides no technical advantages, and there have been many displays and hardware that read in both directions. Further, depending on the nature of the memory and computer (e.g. whether or not the system was big-endian or little-endian), it might be read in reverse order anyway. Therefore, this limitation is meaningless.

As to proof of both of the above, see Giloi (Wolfgang K. Giloi. "Interactive Computer Graphics: Data Structures, Algorithms, Languages". Pages 246-248). Further see Broemmelsiek (US 5,574,836)(7:1-12, 18:62-19:10) and Hannah (US 5,345,252)(2:3-15,7:65-8:67) for proof that both of the above are old and well known in the art.

As to the limitation that "in a time period in which the sprite pattern data is not written to the first storage, the display controller starts to read..." the display **must**

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operate in the manner specified above. It is inherent to the operation of a CRT that the display controller will read data at a given timing, and in CRTs, the data is pulled from the frame buffer, regardless of what the first storage is doing. (Also, there are enablement problems with this wording, see above – it does not make sense that the display would read only when the sprite patterns are not written into the first storage). But in any case, it is an obvious expedient that whenever there is bus latency, that data should be transferred in order to maximize use of the bus and available resources. Obviously, transmitting the data in this 'down time' is old and well known in the art.

Therefore, the limitations of the above claim are met by the instant references and/or are rendered obvious, and/or shown to be implemented (or probably implemented) in holdings of inherency with respect to elements of the already-cited references.

Claim 10 is rejected under 35 U.S.C. 103(a) as unpatentable over Blossom, Yamashita, and Takahashi as applied to claim 6, and further in view of Kitahara et al (US 5,634,850).

As to claim 10,

An image processing device according to claim 6, wherein the prescribed processing correspond to rendering actualizing at least one of magnification, reduction, rotation, and deformation with respect to the sprite pattern data.

Blossom, Yamashita, and Takahashi do not expressly teach that the prescribed processing corresponds to such operations as above. Kitahara, an analogous art (directed to rendering sprites and the like, see Figure 1 with the sprite engine, and the

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Abstract), clearly teaches that the sprite engine clearly reads out image data (such as a character) and carries out processes for the read images such as rotation, enlargement, reduction, and/or color compensation processes (3:59-63), thusly proving that it is obvious to perform such processing when such data is transferred from the first storage to the second storage, since Kitahara initially stores sprites in sprite VRAM 22, and then performs such transformation processing before the data is transferred to sprite frame buffer 23 which is known to hold at least one picture (e.g. frame buffer) – see 3:25-30 and 3:59-63, which when read means that characters are read out of the sprite VRAM 22 (first storage), processed, and sent to sprite frame buffer 23 (second storage) – see Figure 12 or 1 for example.

It would have been obvious to one of ordinary skill in the art to combine the system of Kitahara with Blossom, Yamashita, and Takahashi, since Kitahara provides a more efficient way for processing motion in a system employing sprites (1:50-67).

Claim 11 is rejected under 35 U.S.C. 103(a) as unpatentable over Blossom, Yamashita, Takahashi, and Bromley as applied to claim 7, and further in view of Kitahara et al (US 5,634,850).

As to claim 11,

An image processing device according to claim 6, wherein the prescribed processing correspond to rendering actualizing at least one of magnification, reduction, rotation, and deformation with respect to the sprite pattern data.

Blossom, Yamashita, Takahashi, and Bromley do not expressly teach that the prescribed processing corresponds to such operations as above. Kitahara, an

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analogous art (directed to rendering sprites and the like, see Figure 1 with the sprite engine, and the Abstract), clearly teaches that the sprite engine clearly reads out image data (such as a character) and carries out processes for the read images such as rotation, enlargement, reduction, and/or color compensation processes (3:59-63), thusly proving that it is obvious to perform such processing when such data is transferred from the first storage to the second storage, since Kitahara initially stores sprites in sprite VRAM 22, and then performs such transformation processing before the data is transferred to sprite frame buffer 23 which is known to hold at least one picture (e.g. frame buffer) – see 3:25-30 and 3:59-63, which when read means that characters are read out of the sprite VRAM 22 (first storage), processed, and sent to sprite frame buffer 23 (second storage) – see Figure 12 or 1 for example.

It would have been obvious to one of ordinary skill in the art to combine the system of Kitahara with Blossom, Yamashita, Takahashi, and Bromley, since Kitahara provides a more efficient way for processing motion in a system employing sprites (1:50-67).

### ***Conclusion***

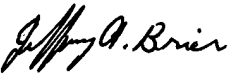
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric V. Woods whose telephone number is 571-272-7775. The examiner can normally be reached on M-F 7:30-4:30 alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 571-272-7664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Eric Woods

  
JEFFERY BRIER  
PRIMARY EXAMINER

14 September 2005